REMARKS

Claims 1 and 8 have been amended. Claims 1-8 are pending in the present application. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claims 1, 3 and 5 stand rejected under 35 U.S.C. § 103 as being unpatentable over Abramson in view of Wunderlich. The rejection is respectfully traversed.

Claim 1 recites an "arbitration method for operating a bus bridge which interfaces a primary-side bus with a plurality of secondary side buses." The bus bridge supports a plurality of kinds of operations, "one of which is an operation related to a serial bus in accordance with IEEE1394." The claimed method operates the bus bridge by "giving an access right equally to each of the secondary-side buses, when access demands to the primary-side bus are lodged from more than two of the secondary-side buses at the same time, by not giving a priority to any one of the secondary-side buses." According to claim 1, "a counter is used such that access rights are provided sequentially to the more than two secondary-side buses lodging access demands and at a same rate of the lodged access demands."

Applicant respectfully submits that Abramson and Wunderlich, even when considered together, fail to teach or suggest the claimed invention. As noted in the Office Action, Abramson fails to teach or suggest an arbitration method in which the bus bridge supports a serial bus in accordance with IEEE 1394. To overcome the deficiency, the Office Action now relies on Wunderlich. Wunderlich discloses a computer system having bridge logic that couples peripheral devices to a CPU and main memory. The bridge logic has power management logic to adjust the CPU's internal clock in accordance with the general activity level of the computer. Wunderlich Col. 3, ll. 56-62. The bridge logic is a "south bridge" that connects to the

CPU via a "north bridge" and an expansion bus. Wunderlich Col. 4, ll. 10-13. The expansion bus could include an IEEE 1394 bus or a USB bus. The goal of the Wunderlich system is to save "as much battery power as possible." Wunderlich Col. 6, ll. 12-13. Applicant respectfully submits that Wunderlich does not teach or suggest an arbitration method for a system having an IEEE 1394 bus.

The combination of Abramson and Wunderlich fails to teach or suggest an arbitration method where "access rights are provided sequentially to the more than two secondary-side buses lodging access demands and at a same rate of the lodged access demands" as recited in claim 1.

Abramson, by contrast, discloses a Host Bridge 115, a BIU 140, a USB 150 and 155, a PCI bus 130, a memory 120, and an arbitration method between two USBs. A USB arbiter couples a first USB host controller and the second USB host controller to a bus. The arbiter arbitrates between grant request signals from the first and second USB host controllers. As such, Abramson does not teach or suggest arbitration between "more than two" secondary-side buses as is recited in claim 1. Applicant respectfully submits that neither does Wunderlich. Thus, for at least this reason, the combination of Abramson and Wunderlich fails to disclose, teach or suggest the claimed method.

Moreover, Abramson fails to disclose, teach or suggest an arbitration method where "a counter is used such that access rights are provided sequentially to the more than two secondary-side buses lodging access demands and at a same rate of the lodged access demands." Abramson, by contrast, discloses two arbitration techniques. The first technique is a ping-pong state machine method illustrated in Abramson's Figures 2A (reproduced on the next page) and 2B. According to Abramson:

> In a first state 202, the priority solver assigns a higher priority to first USB host controller 150 such that when a

contention occurs, first USB host controller 150 will receive the grant. After first USB host controller 150 is granted access to the bus, state machine 200 transitions along transition path 204 to second state 208. USB priority solver state machine 200 remains in second state 208 until USB arbiter 145 grants second USB host controller 155 access to PCI bus 130. After second USB host controller 155 receives access to PCI bus 130, priority solver state machine 200 transitions along transition path 210 to initial state 202 wherein the first USB host controller 150 again has priority.
[Abramson Col. 4, ll. 4-16.]

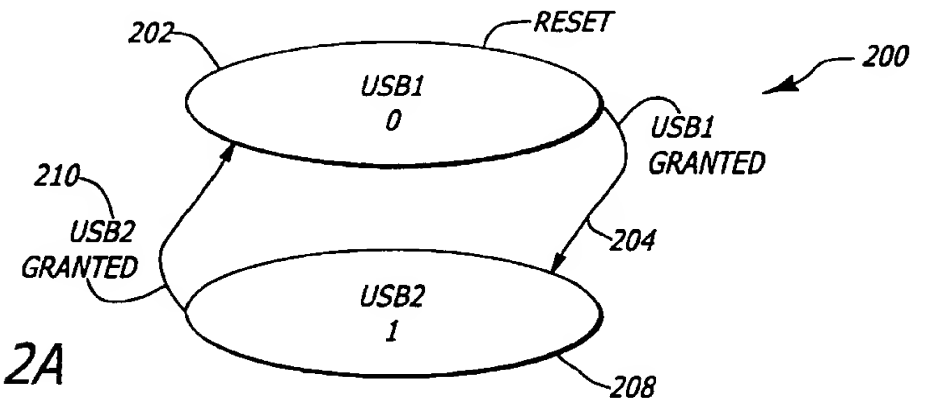

FIG. 2A

As such, access is ping-ponged between a first USB controller and a second USB controller. This is not the same as the claimed invention because it can not provide access rights "sequentially to the more than two secondary-side buses lodging access demands and at a same rate of the lodged access demands" as required by claim 1.

The second Abramson technique, relied upon by the Final Rejection and the Advisory Action, is a "rotating arbitration" scheme that "selects subsequent USB host controllers in a predetermined sequence." Abramson, Col. 5, ll. 29-31. This rotating arbitration method maintains a strict order in which access rights are to be granted (i.e., USB controller 1, controller 2, controller 1, controller 2, controller 1, etc.). This is not the same as the claimed invention because it can not provide access rights "sequentially to

the more than two secondary-side buses lodging access demands and at a same rate of the lodged access demands" as required by claim 1. Furthermore, Abramson fails to disclose, teach or suggest a "counter" that is used such that "access rights are provided sequentially to the more than two secondary-side buses lodging access demands and at a same rate of the lodged access demands."

Moreover, Applicant respectfully submits that Wunderlich does not teach or suggest an arbitration method where "a counter is used such that access rights are provided sequentially to the more than two secondary-side buses lodging access demands and at a same rate of the lodged access demands." In fact, Wunderlich does not teach any arbitration method at all. Thus, the combination of Wunderlich and Abramson fail to teach or suggest the same limitation of claim 1. Accordingly, claim 1 is allowable over the cited combination.

Claims 3 and 5 depend from claim 1 and are allowable along with claim 1. The rejection should be withdrawn and the claims allowed.

Claims 2, 4 and 8 stand rejected under 35 U.S.C. § 103 as being unpatentable over Abramson in view of Wunderlich and further in view of Tang. The rejection is respectfully traversed.

Claims 2 and 4 depend from claim 1 and thus recite "a counter [that] is used such that access rights are provided sequentially to the more than two secondary-side buses lodging access demands and at a same rate of the lodged access demands." As set forth above, this is not disclosed, taught or suggested by the combination of Abramson and Wunderlich. Applicant respectfully submits that Tang, which has been cited merely for teaching card buses, fails to teach or suggest the limitation as well. As such, claims 2 and 4 are allowable for at least the reasons set forth above.

Claim 8 also recites "wherein said system further comprises a counter such that access rights are provided sequentially to the more than two secondary-side buses lodging access demands and at a same rate of the lodged access demands." As such, claim 8 is allowable for at least the reasons set forth above.

Claims 6 and 7 stand rejected under 35 U.S.C. § 103 as being unpatentable over Abramson in view of Wunderlich and further in view of Quackenbush. The rejection is respectfully traversed.

Claim 6 depends from claim 1 and thus recites "a counter is used such that access rights are provided sequentially to the more than two secondary-side buses lodging access demands and at a same rate of the lodged access demands." As set forth above, this is not disclosed, taught or suggested by the combination of Abramson and Wunderlich. Applicant respectfully submits that Quackenbush, which has been cited merely for teaching a PCI bus, fails to teach or suggest this limitation as well. As such, claim 6 is allowable for at least the reasons set forth above.

Claim 7 recites an "arbitration method of a bus bridge which interfaces a primary-side bus with a plurality of secondary-side buses" where the primary side bus is "a local bus in a system and the secondary-side buses being external buses connected to the system." According to claim 7, "at least one of the secondary-side buses [is] a serial bus in accordance with IEEE 1394." The arbitration method comprises the step of "giving a highest priority to the primary-side bus when the primary side bus lodges an access demand to the secondary-side buses irrespective of a condition of an arbitration between the secondary-side buses."

The combination of Abramson, Wunderlich and Quackenbush does not teach or suggest the recited method because the references do not arbitrate between a

primary bus, at least one IEEE 1394 bus and at least one other bus. As set forth above and in Applicant's prior Amendment, the references fail to teach or suggest an arbitration method for a serial bus in accordance with IEEE 1394. As such, they fail to account for the distinct difference in access requirements between a USB and IEEE 1394 serial bus. One such difference is the access time required for data transfer using an IEEE 1394 serial bus. Accordingly, a problem when using an IEEE 1394 serial bus is that it can prevent access rights from being granted to other secondary side buses. This problem is not fully appreciated by Abramson or the other references. Abramson merely has a register that limits the time a host controller can spend on the bus as an initiator and fails to teach or suggest the requirements needed to arbitrate between buses that are not USB buses. Abramson Col. 3, lines 34-36. In addition, USB buses do not support the same devices used by an IEEE 1394 bus. Therefore, the rejection should be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: November 30, 2004

Respectfully submitted,

By_____

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